REMARKS

Claims 1, 2, 4 - 8, and 15-18 are pending.

A Non Final Office Action dated November 14, 2005 and a Final Office Action dated May 16, 2005, preceded an Advisory Action dated August 3, 2006.

Claims 1, 2, 4 – 5, and 15 stand rejected under 35 USC § 102(e) as being anticipated by US patent publication No. 2002/0175846 (hereinafter referred to as "the Sakimura application"). Claims 1, 4, 8, 17 and 18 stand rejected under 35 USC §102(b) as being anticipated by US Patent No. 6,407,685 (hereinafter referred to as "the Händel patent"). Claims 6 – 7, 16 and 17 also stand rejected under 35 USC § 102(a) as being anticipated over the Händel patent as applied to Claims 1, 3 and 4, and in view of Applicant Admitted Prior Art (AAPA).

Claim 1 recites a <u>continuous time</u> sigma delta converter that comprises conversion means having known non-ideal characteristics. Claim 4 recites a method of compensating for known non-ideal characteristics in a <u>continuous time</u> sigma delta converter. Claims 2, 5 – 8 and 15 - 18 depend from claim 1. The feature of a continuous time sigma delta converter is not disclosed in the cited prior art.

For this Statement, Applicants will be focusing on two specific points:

1) that the Sakimura application does not teach a continuous time sigma-delta converter; and

2) that the Händel patent does not teach a continuous time sigma-delta converter.

<u>1) The Sakimura application does not teach a continuous time sigma-delta converter</u>

Page 7, paragraph [0100] to page 8, paragraph [0101], of the Sakimura application describes a circuit configuration that addresses quantization noise leakage in analog integrators 2a, 2b due to non-linearities of a D/A converter 6.

The Sakimura application does not teach "a <u>continuous time</u> sigma delta converter" as recited in Claim 1. The Sakimura application discloses, for example in relation to FIG. 5, the first and second analog integrators 2a, 2b operating in the z-domain, operation in the z-domain being indicative that the conversion means of FIG. 5 is discrete time in nature. If the Sakimura application wanted to make specific reference to continuous time operation, then reference would have been made to the <u>s</u>-domain. The Sakimura application explicitly refers to the z-domain, but not the s-domain and, in conjunction with common general knowledge in the

technical field, it is submitted that reference to the z-domain unambiguously teaches discrete-time operation. Indeed, this is the view of the Inventor (Applicant's technical expert).

The Advisory Action states that Fig. 3 of Sakimura clearly discloses a continuous conversion signal of sigma-delta A/D with respect to time.

Applicants respectfully disagree for the following reasons.

FIG. 3 actually teaches discrete-time operation. A conclusion of continuous-time operation seems to have been reached from a brief visual inspection of the waveforms shown. However, as would be appreciated by the skilled person, the level of magnification is not sufficiently great to show the true nature of the waveforms. It is therefore submitted that if one were to observe the waveforms of FIG. 3 at a greater level of magnification, one would see that the relevant signals are, in fact, discrete-time signals. This is the true nature of the signals of Fig. 3. Furthermore, as evidenced by the first 4 lines of paragraph [0096] and paragraph [0137], page 11, lines 4-7, the sigma-delta converters described in the Sakimura application are implemented using switched capacitor circuits. In this respect, it is very clear that use of switched capacitor circuits operate in a discrete-time mode. Therefore, the Sakimura application discloses a discrete time sigma delta modulator, which is not the same as the continuous time sigma delta converter.

2) The Händel patent does not teach a continuous time sigma-delta converter

The Händel patent discloses a Nyquist rate ADC. FIG. 4A of the Händel patent shows an exemplary ADC and an associated calibrator (col. 8, lines 11-13). FIG. 4B shows exemplary details of an embodiment of calibration logic (col. 8, lines 35-37), and FIG. 4C shows another exemplary embodiment of calibration logic for the ADC (col. 9, lines 31-33).

The Advisory Action states that Handel et al. Col. 5, line 25, discloses a continuous time A/D converter, and that lines 44 - 47 discloses an A/D converter as a sigma-delta converter.

Applicants respectfully disagree for the following reasons.

Col. 5, line 25 simply explains that the ADC 105 converts a time-continuous and amplitude-continuous signal to a time-discrete and amplitude-discrete signal. This is true of all ADCs (as well as sigma-delta converters irrespective of whether they are continuous-time or discrete-time in nature). Likewise, col. 5, lines 35-38 simply explains that the ADC quantizes each sampled analog input signal into one of finite number of levels and represents each level a

bit pattern. Col. 5, lines 42-48 simply explains that the principles of the invention disclosed in the Händel patent are applicable to other ADC environments, namely a sigma-delta ADC.

However, FIGS. 4A, 4B and 4C, and the above cited passages from col. 5 of the Händel patent, do not teach a "continuous time sigma-delta converter" as recited in claim 1. In this respect, col. 5, lines 42-48 are <u>completely silent as to the nature of the sigma-delta converter</u>. Indeed, col. 5, lines 42-48 simply explains that the principles of the invention of the Händel patent, namely the provision of the calibrator, can be employed in a sigma-delta ADC. Hence, the Händel patent <u>does not actually disclose</u> a sigma-delta ADC possessing the features recited in Claim 1, only that a particular inventive principle, namely calibration, can be applied to sigma-delta ADCs. This statement is made, <u>in passing</u>, in the Händel patent and is <u>very ambiguous</u>. The passages relied upon in Section 5 of the Office Action relate to FIGs. 4A, 4B and 4C of the Händel patent. In this respect, the ADCs employed in FIGs. 4A, 4B and 4C are <u>Nyquist rate ADCs</u>. Nyquist rate ADCs are <u>very different</u> to sigma-delta converters, because sigma-delta converters employ over-sampling, i.e. rates far greater than the Nyquist rate. Additionally, a sigma-delta converter comprises a very different architecture to that of a Nyquist rate ADC, which possess sample and hold circuitry. Continuous time sigma-delta converters, in contrast, <u>do not employ sample and hold circuitry</u> in order to achieve the continuous nature of the mode of operation. <u>Consequently, the Händel patent only relates to discrete-time circuits</u>, and in particular with reference to FIGs. 4A, 4B and 4C, addresses non-linearities of Nyquist rate ADCs, which are, of course, discrete-time circuits. The nature of the input signal and the output signal in terms of whether or not they are continuous-time or discrete-time is not relevant in assessing whether <u>a circuit itself</u> is a continuous-time or discrete-time sigma-delta converter.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By: /David G. Dolezal/
David G. Dolezal
Attorney of Record
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6854